IN THE CLAIMS

Please cancel claim 19, and amend claims 1, 7, 13, and 20 as indicated below.

1. (Currently Amended) A method for testing comprising:
   storing a first value of a first pattern in a register;
   storing a second value of a second pattern in the register;
   receiving a clock signal;
   selecting either said first value or said second value for inclusion in a test pattern for conveyance via a link in response to said clock signal;
   wherein determining whether to select either said first value or said second value on a given clock cycle is determined according to a predetermined test pattern sequence; and
   wherein said register comprises N bits, said first pattern comprises N/2 bits, said second pattern comprises N/2 bits, and said link comprises N/2 signal lines, and wherein each signal line corresponds to one bit of each of said first pattern and said second pattern.

2. (Original) The method as recited in claim 1, wherein said test pattern sequence comprises a plurality of indications, each of said indications indicating either said first value or said second value.

3. (Original) The method as recited in claim 2, wherein said first value is stored in a first register location, and said second value is stored in a second register location, and wherein both said first and second register locations correspond to a same link signal line.

4. (Original) The method as recited in claim 3, further comprising driving values of said test pattern from a first component to a second component.

5. (Original) The method as recited in claim 4, wherein each of said first component

and said second component alternate driving values of said test pattern during a sixteen test cycle sequence.

6. (Previously Presented) The method as recited in claim 5, wherein said alternate driving of values by said first component and said second component is separated by one or more turn-around cycles.

7. (Currently Amended) A system comprising:
a first component;
a second component; and
a link coupling said first component to said second component;
wherein said first component is configured to:
determine whether to select either a first stored value of a first pattern in a register or a second stored value of a second pattern in a register for inclusion in a test pattern on a given clock cycle, wherein said determination is based upon a predetermined test pattern sequence;
wherein said register comprises N bits, said first pattern comprises N/2 bits, said second pattern comprises N/2 bits, and said link comprises N/2 signal lines, and wherein each signal line corresponds to one bit of each of said first pattern and said second pattern.

8. (Original) The system as recited in claim 7, wherein said predetermined test pattern sequence comprises a sequence of sixteen indications, each of said indications indicating either said first value or said second value.

9. (Original) The system as recited in claim 8, wherein said link comprises a signal line, and wherein said first value is stored in a first register location, and said second value is stored in a second register location, and wherein both said first and second register locations correspond to a same link signal line.

10. (Original) The system as recited in claim 9, wherein said first component is

configured to drive values of said test pattern to said second component.

11. (Original) The system as recited in claim 10, wherein each of said first component and said second component alternate driving values of said test pattern during a sixteen indication test cycle sequence.

12. (Previously Presented) The system as recited in claim 10, wherein each of said first component and said second component alternate driving values of said test pattern during a sixteen test cycle sequence, wherein each of said components drives two consecutive values in turn.

13. (Currently Amended) A component comprising:

a plurality of drivers, each of said drivers coupled to a separate signal line of a plurality of signal lines of a link;

a register configured to store a first bit pattern and a second bit pattern, wherein each bit of said first bit pattern and said second bit pattern corresponds to a signal line of said link;

a test pattern sequence unit, wherein said unit is configured to indicate a predetermined sequence in which values are to be selected from either said first bit pattern or said second bit pattern; and

control circuitry configured to generate a test pattern, wherein on a given test cycle said circuitry is configured to select a value from either said first bit pattern or said second bit pattern in response to detecting an indication in said test pattern sequence which indicates one of said first bit pattern and said second bit pattern is to be accessed;

wherein said register comprises N bits, said first pattern comprises N/2 bits, said second pattern comprises N/2 bits, and said link comprises N/2 signal lines, and wherein each signal line corresponds to one bit of each of said first pattern and said second pattern.

14. (Original) The component as recited in claim 13, wherein said predetermined test

pattern sequence comprises a plurality of indications, each of said indications indicating either said first value or said second value.

15. (Original) The component as recited in claim 14, wherein each test cycle said control circuitry iterates through said test pattern sequence in order to ascertain a bit pattern indication for each test cycle.

16. (Original) The component as recited in claim 15, wherein said component is configured to drive values of said test pattern via said link.

17. (Original) The component as recited in claim 16, wherein during a sixteen test cycle sequence, said component is configured to alternate between driving two sequential values of said test pattern and receiving two values of said test pattern.

18. (Original) The component as recited in claim 13, further comprising a plurality of receivers coupled to said link, and wherein said component includes pattern checking circuitry configured to compare values received via said link to expected values.

19. (Cancelled).

20. (Currently Amended) The component as recited in claim ~~19~~ 13, wherein each signal line is coupled to receive a value from a multiplexor, wherein each multiplexor is coupled to one bit of said first pattern and one bit of said second pattern, and wherein said control circuitry is configured to control each multiplexor to convey from each multiplexor a bit from either said first pattern or said second pattern.